

FIG. 1

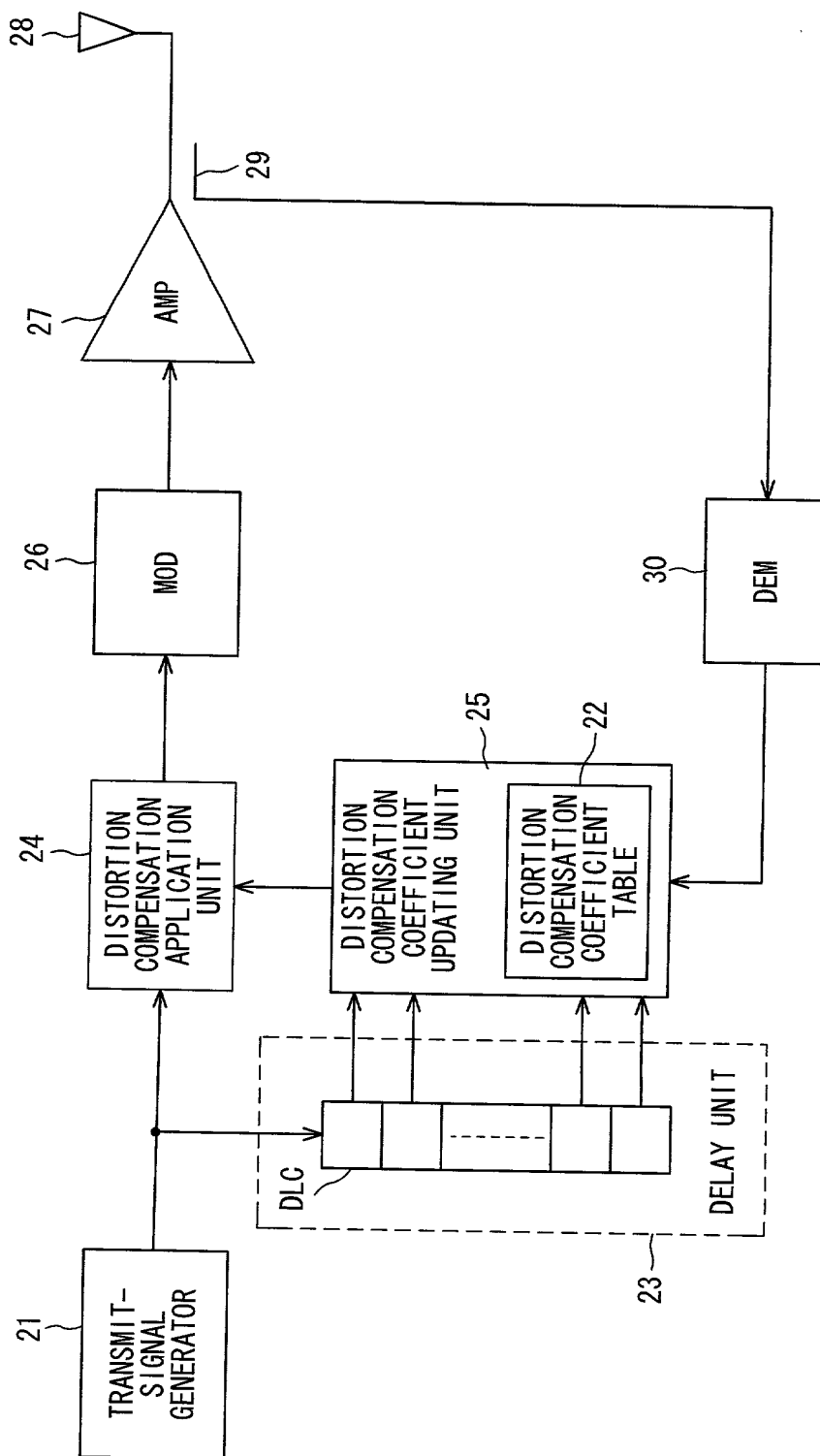
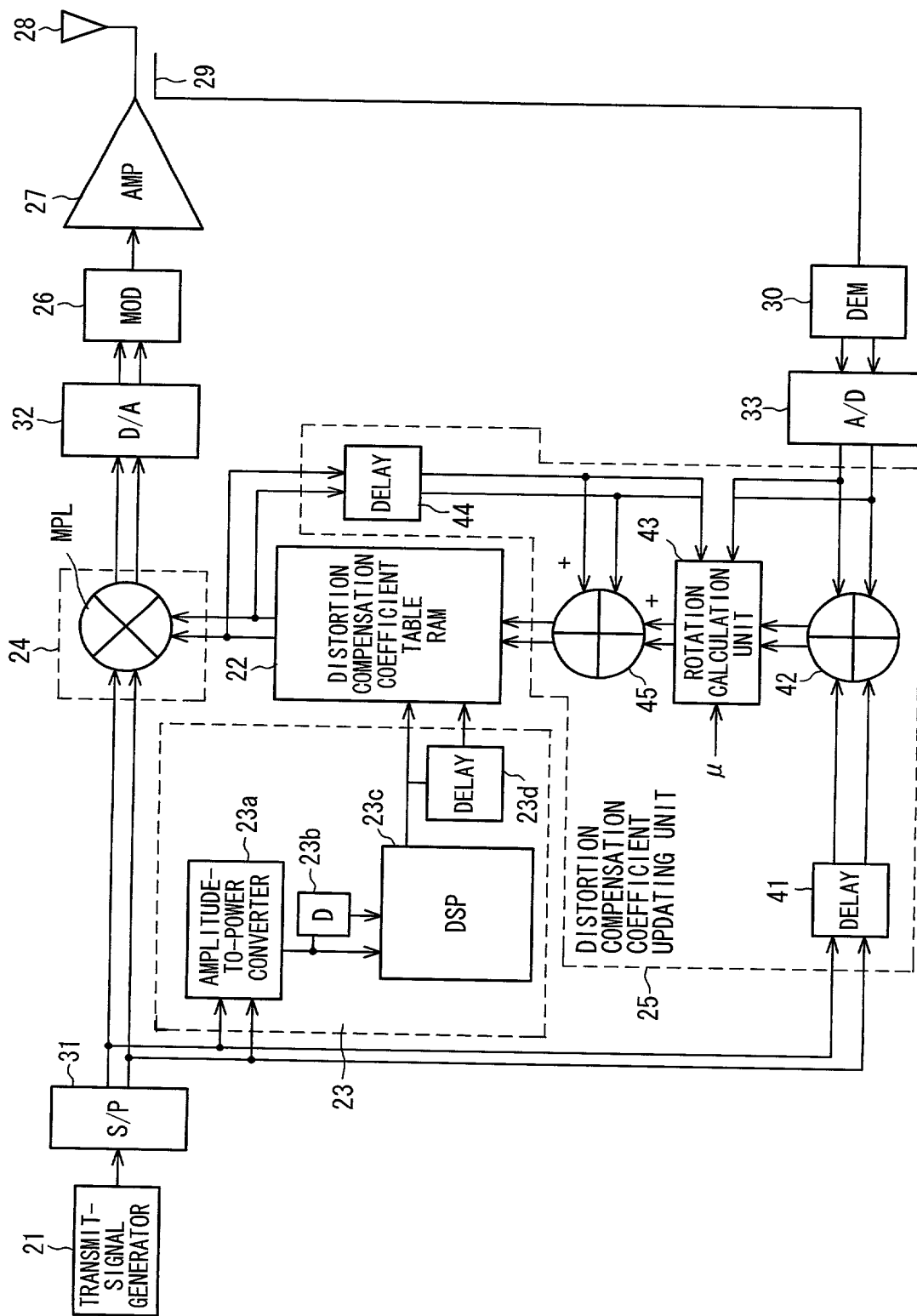


FIG. 2



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FIG. 3

$P(t)$	ΔP	$h(P(t), \Delta P)$
P_1	ΔP_1	$h(P_1, \Delta P_1)$
	ΔP_2	$h(P_1, \Delta P_2)$
	ΔP_3	$h(P_1, \Delta P_3)$
	\vdots	\vdots
	ΔP_n	$h(P_1, \Delta P_n)$
P_2	ΔP_1	$h(P_2, \Delta P_1)$
	ΔP_2	$h(P_2, \Delta P_2)$
	ΔP_3	$h(P_2, \Delta P_3)$
	\vdots	\vdots
	ΔP_n	$h(P_2, \Delta P_n)$
P_3 \vdots	\vdots	\vdots
P_m	ΔP_1	$h(P_m, \Delta P_1)$
	ΔP_2	$h(P_m, \Delta P_2)$
	ΔP_3	$h(P_m, \Delta P_3)$
	\vdots	\vdots
	ΔP_n	$h(P_m, \Delta P_n)$

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FIG. 4

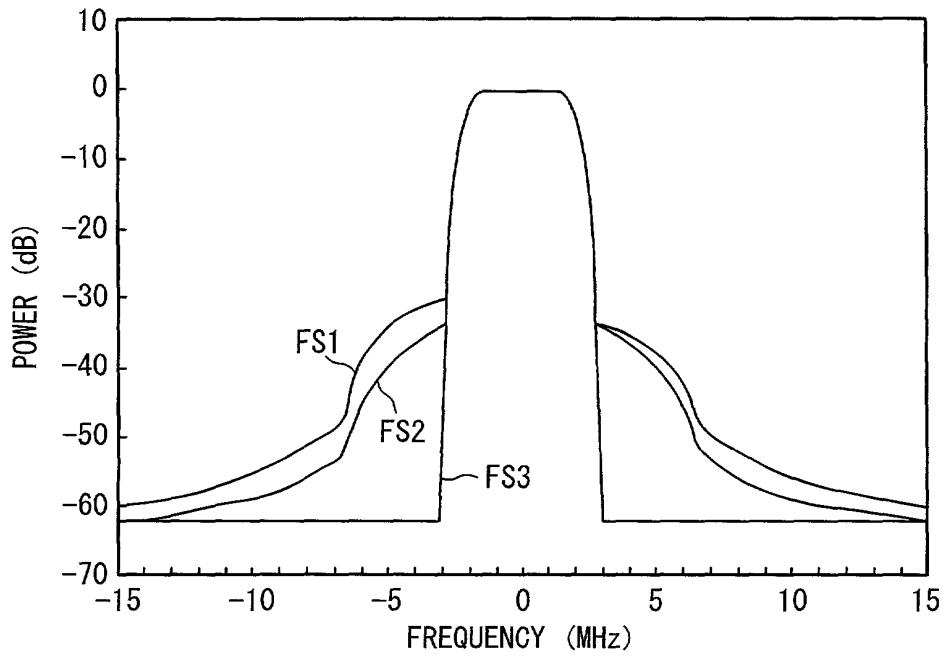


FIG. 5

ITEM	SPECIFICATIONS
CHIP RATE	4.096 Mbps
CARRIER RATE	64 kbps
NUMBER OF MULTIPLEXED SIGNALS	60 CODES
PEAK SUPPRESSION	13.5 CODES
CHIP SHAPING FILTER	ROUTE NYQUIST ($\alpha=0.22$)

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FIG. 6

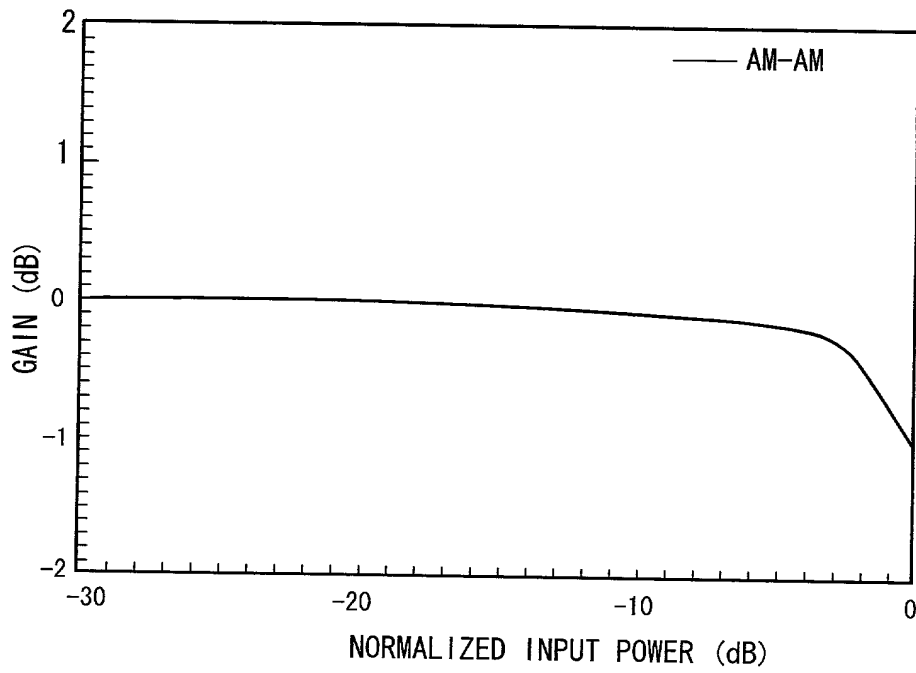
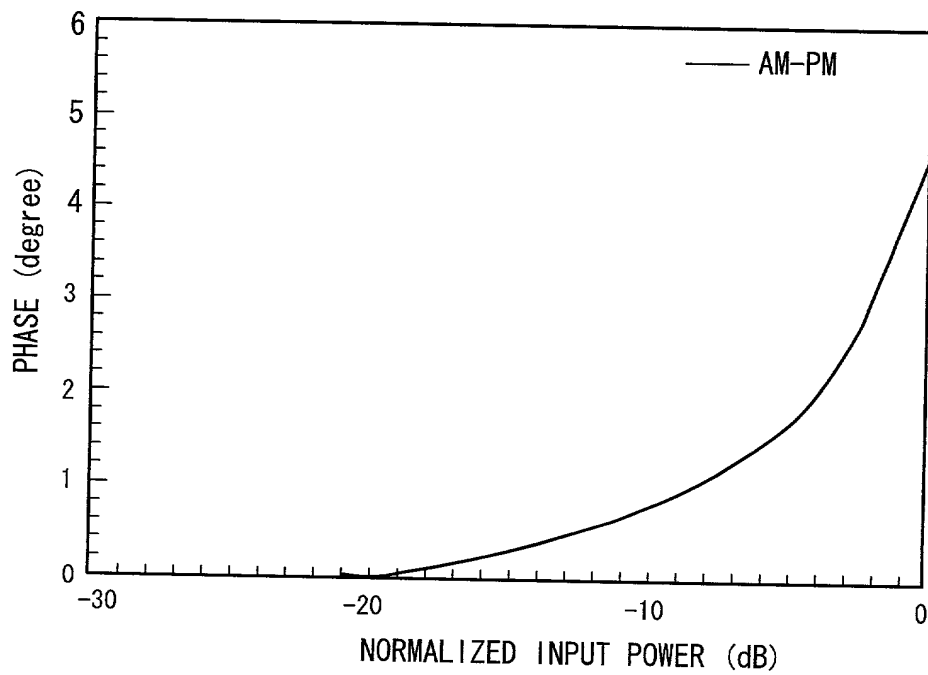


FIG. 7



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FIG. 8

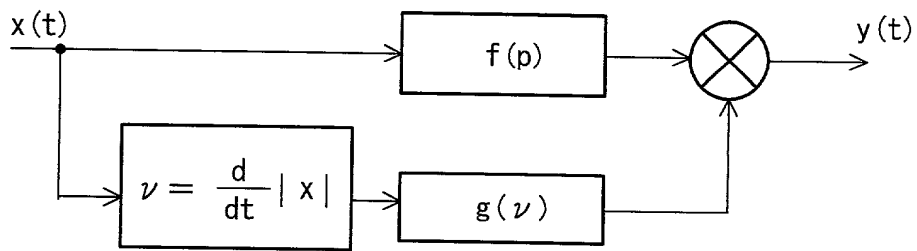
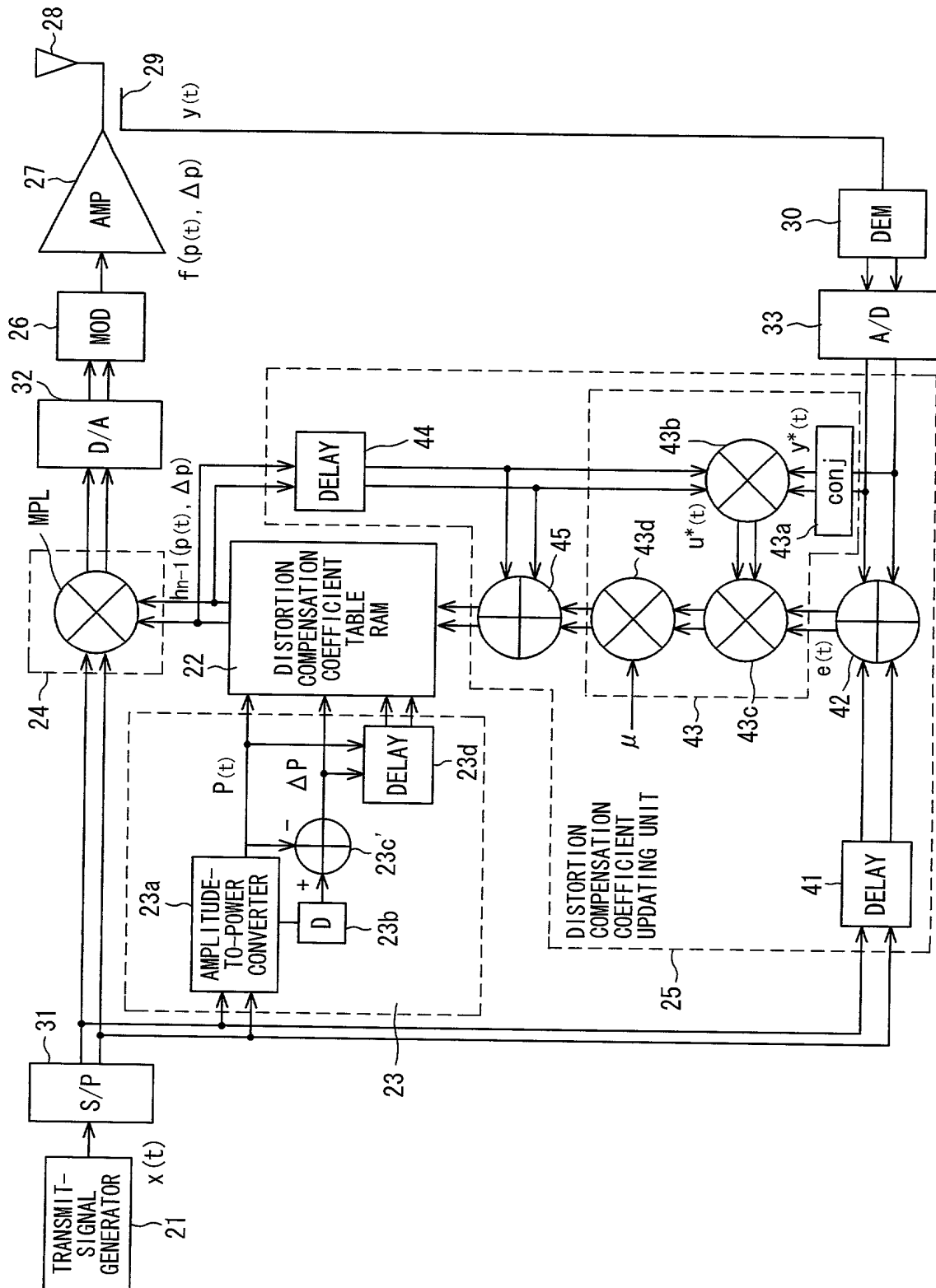


FIG. 9



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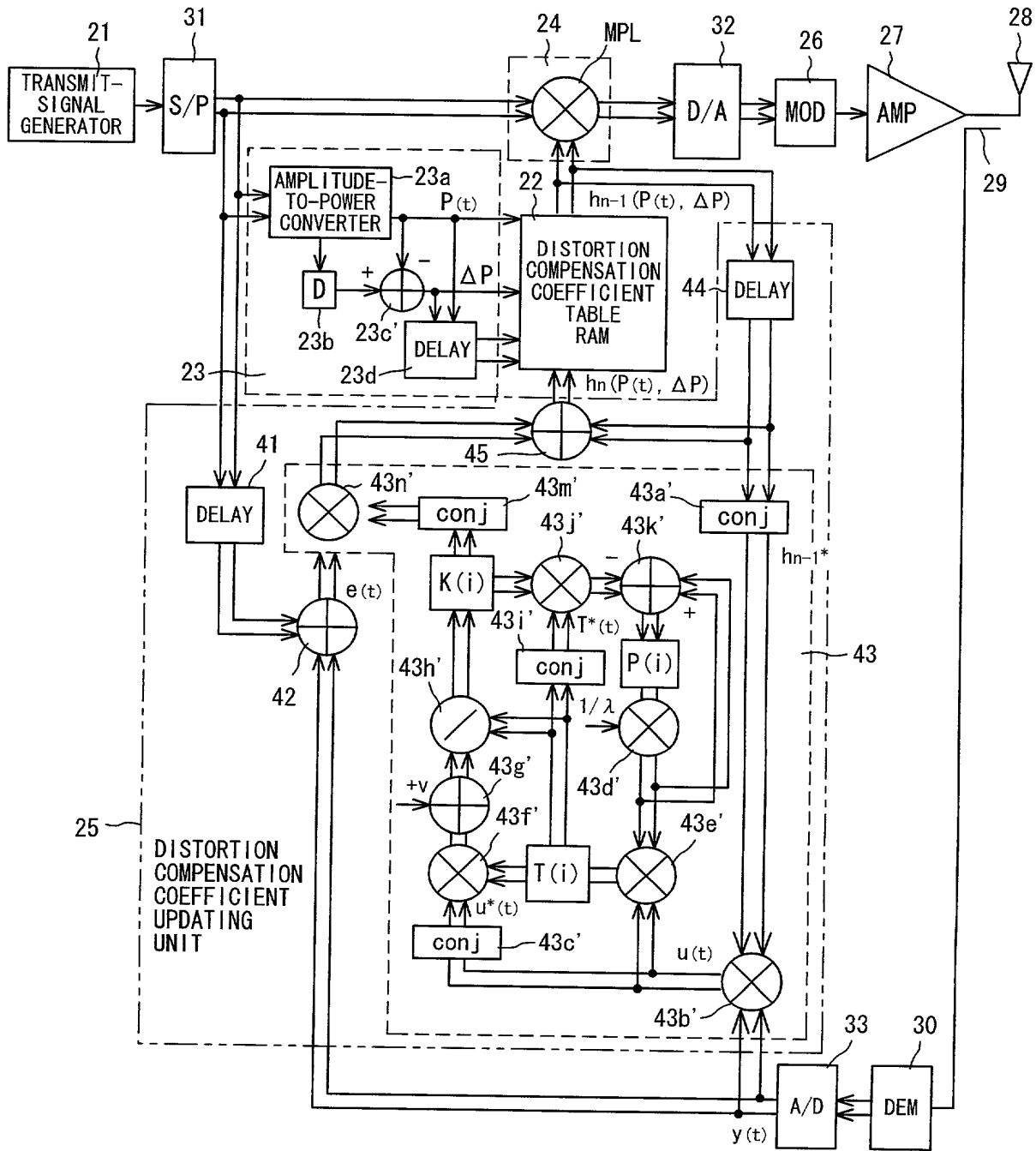
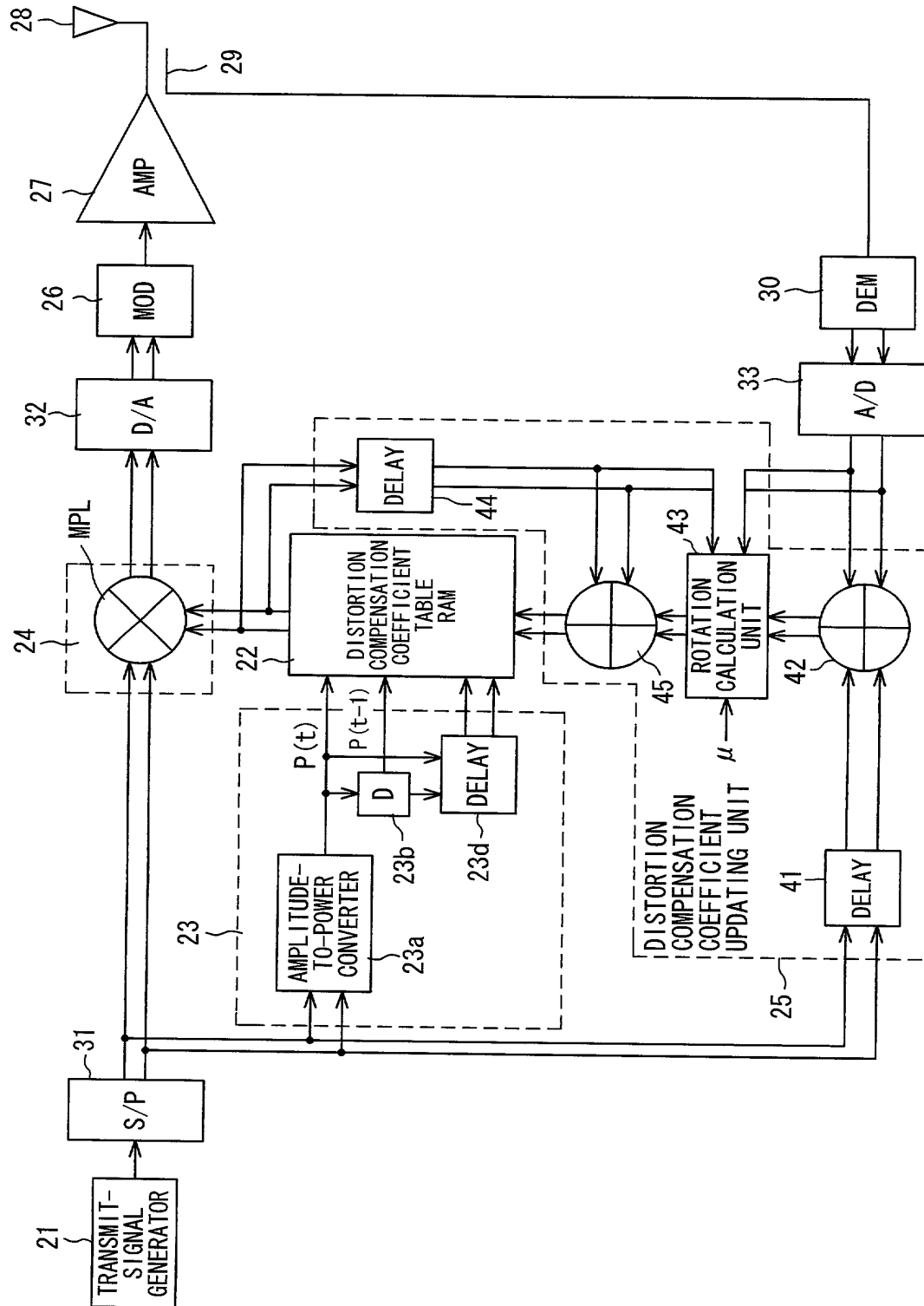
FIG. 10

FIG. 11



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FIG. 12

$P(t)$	$P(t-1)$	$h(P(t), P(t-1))$
P_1	P_1	$h(P_1, P_1)$
	P_2	$h(P_1, P_2)$
	P_3	$h(P_1, P_3)$
	\vdots	\vdots
	P_n	$h(P_1, P_n)$
P_2	P_1	$h(P_2, P_1)$
	P_2	$h(P_2, P_2)$
	P_3	$h(P_2, P_3)$
	\vdots	\vdots
	P_n	$h(P_2, P_n)$
P_3 \vdots	\vdots	\vdots
P_m	P_1	$h(P_m, P_1)$
	P_2	$h(P_m, P_2)$
	P_3	$h(P_m, P_3)$
	\vdots	\vdots
	P_n	$h(P_m, P_n)$

FIG. 13

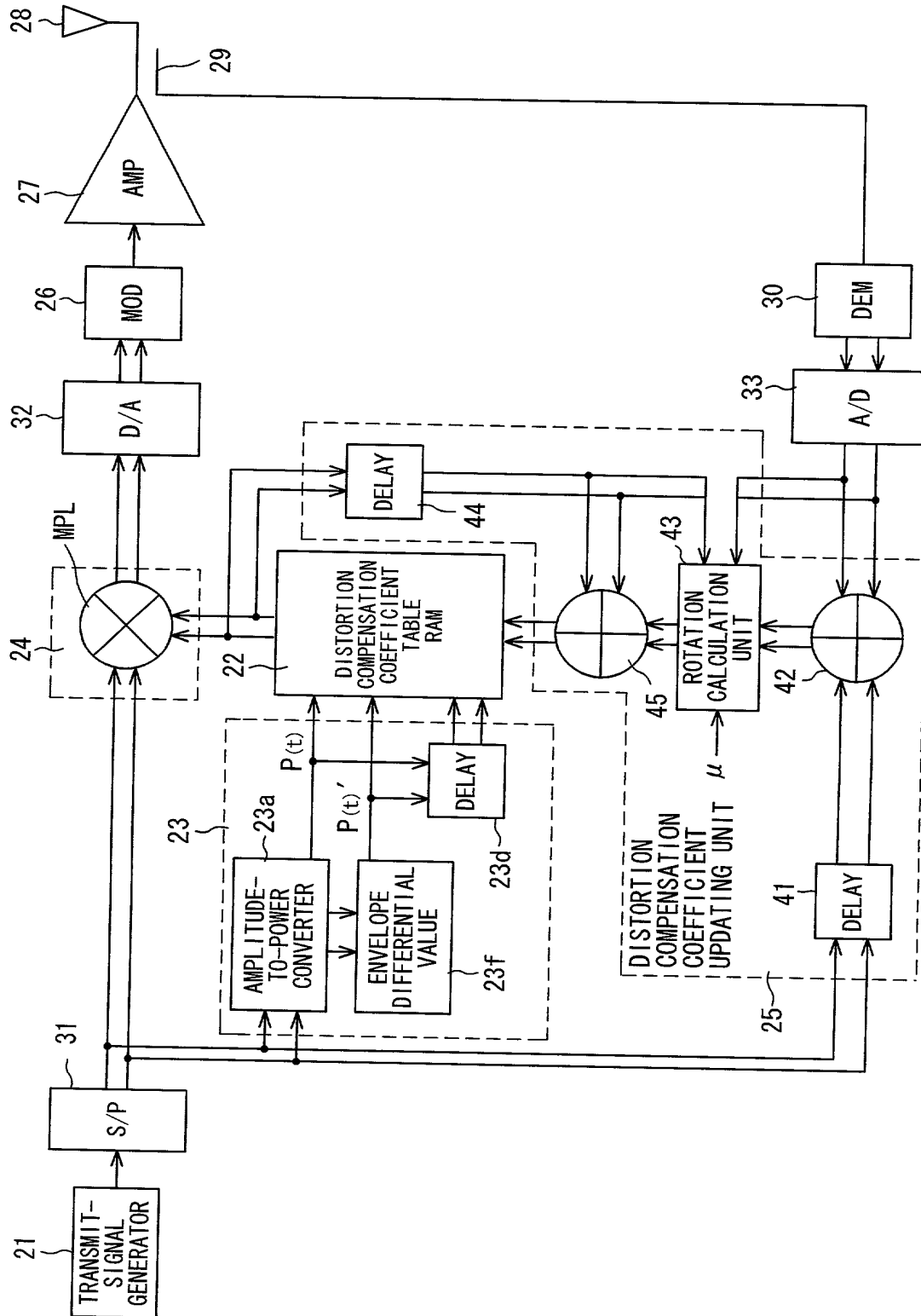


FIG. 14

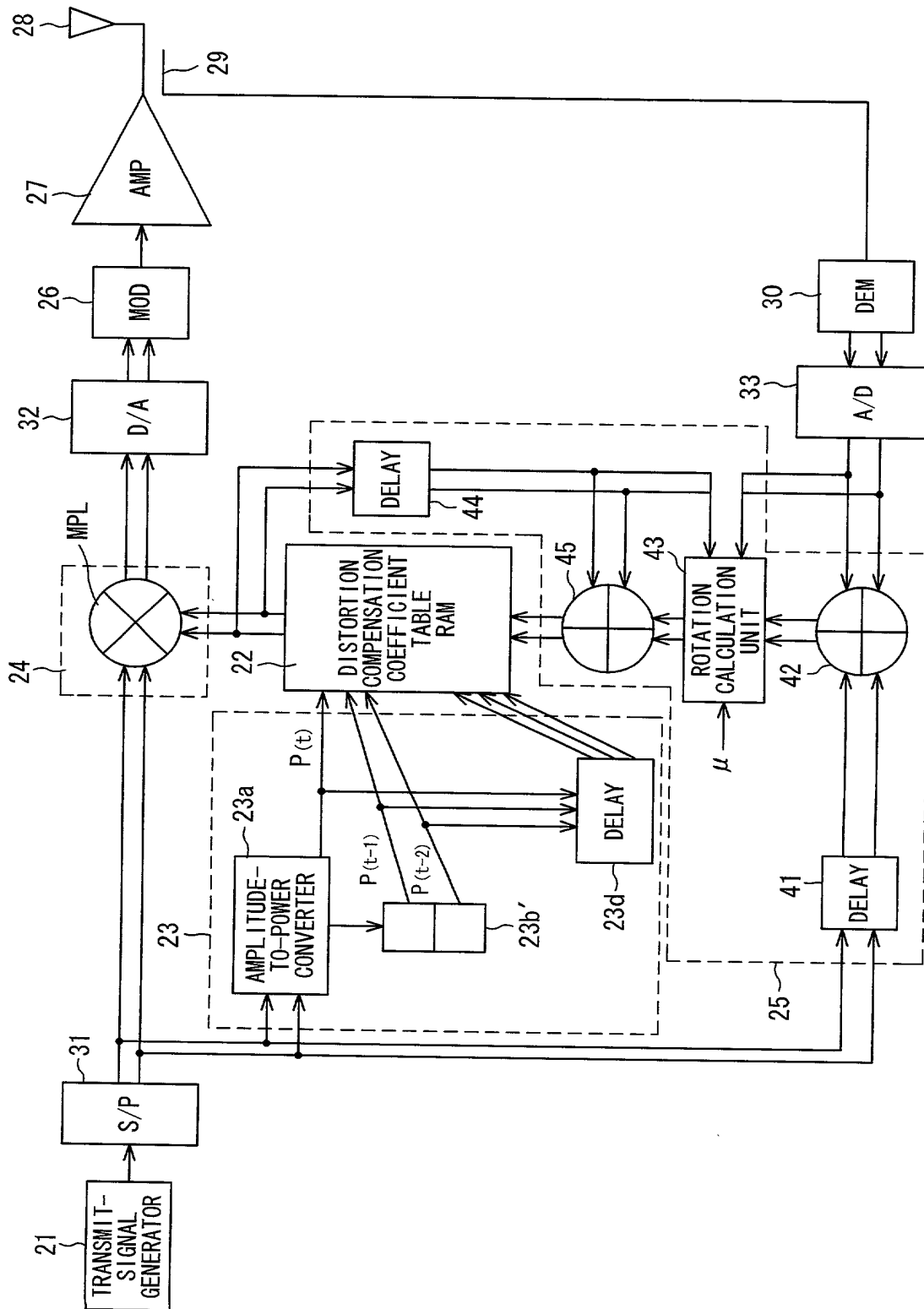
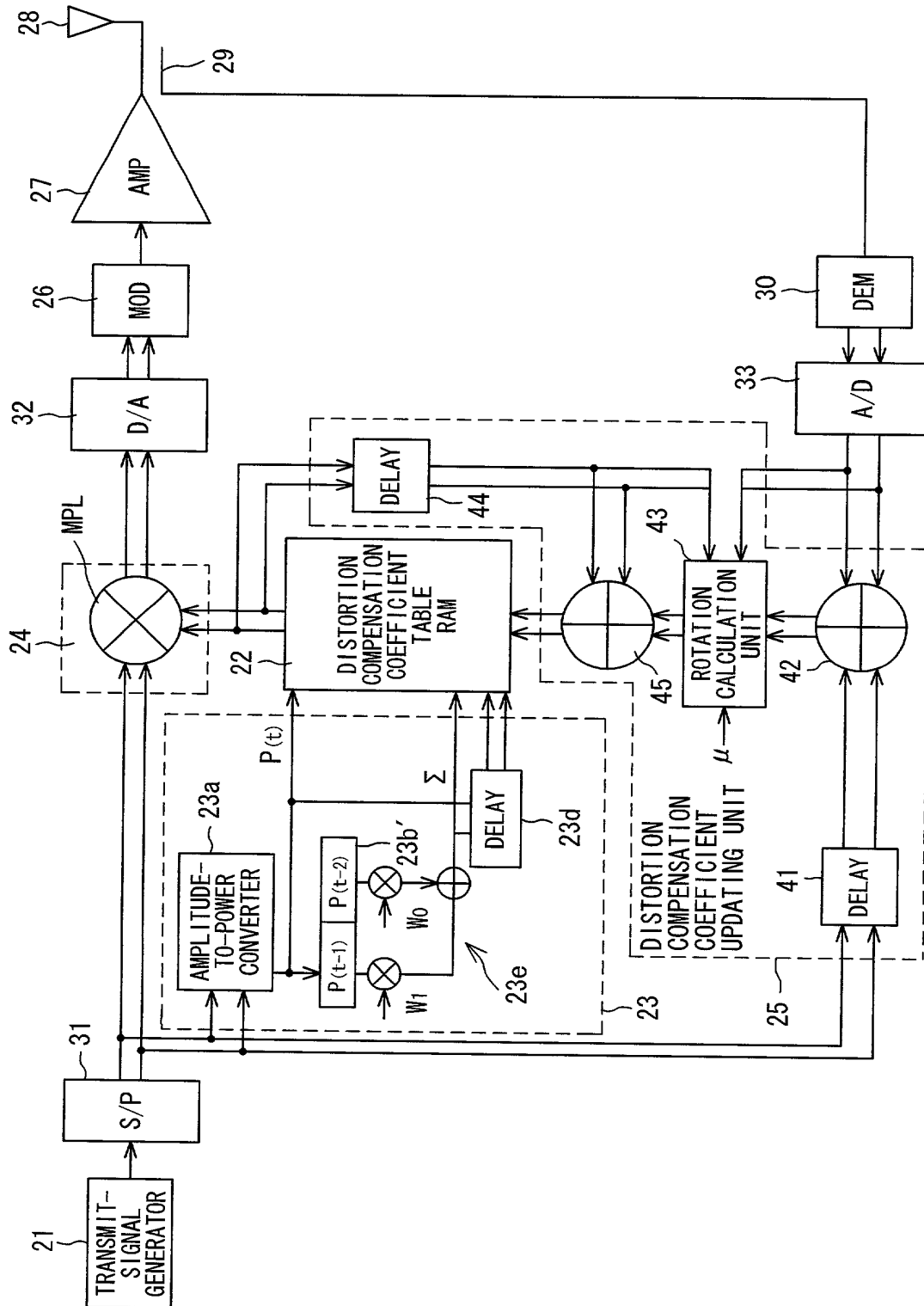


FIG. 15

$P(t)$	$P(t-1)$	$P(t-2)$	$h(P(t), P(t-1), P(t-2))$
P_1	P_1	P_1	$h(P_1, P_1, P_1)$
		P_2	$h(P_1, P_1, P_2)$
		\vdots	\vdots
		P_n	$h(P_1, P_1, P_n)$
	P_2	P_1	$h(P_1, P_2, P_1)$
		P_2	$h(P_1, P_2, P_2)$
		\vdots	\vdots
		P_n	$h(P_1, P_2, P_n)$
	\vdots	\vdots	\vdots
	P_n	P_1	$h(P_1, P_n, P_1)$
		P_2	$h(P_1, P_n, P_2)$
		\vdots	\vdots
		P_n	$h(P_1, P_n, P_n)$
P_2	P_1	P_1	$h(P_2, P_1, P_1)$
		P_2	$h(P_2, P_1, P_2)$
		\vdots	\vdots
		P_n	$h(P_2, P_1, P_n)$
\vdots	P_2		
\vdots	\vdots	\vdots	\vdots
\vdots	\vdots	\vdots	\vdots
P_m			

code	category	code	category	code	category	code	category	code	category
00	000000	00	000000	00	000000	00	000000	00	000000
01	000001	01	000001	01	000001	01	000001	01	000001
02	000002	02	000002	02	000002	02	000002	02	000002
03	000003	03	000003	03	000003	03	000003	03	000003
04	000004	04	000004	04	000004	04	000004	04	000004
05	000005	05	000005	05	000005	05	000005	05	000005
06	000006	06	000006	06	000006	06	000006	06	000006
07	000007	07	000007	07	000007	07	000007	07	000007
08	000008	08	000008	08	000008	08	000008	08	000008
09	000009	09	000009	09	000009	09	000009	09	000009
10	000010	10	000010	10	000010	10	000010	10	000010
11	000011	11	000011	11	000011	11	000011	11	000011
12	000012	12	000012	12	000012	12	000012	12	000012
13	000013	13	000013	13	000013	13	000013	13	000013
14	000014	14	000014	14	000014	14	000014	14	000014
15	000015	15	000015	15	000015	15	000015	15	000015
16	000016	16	000016	16	000016	16	000016	16	000016
17	000017	17	000017	17	000017	17	000017	17	000017
18	000018	18	000018	18	000018	18	000018	18	000018
19	000019	19	000019	19	000019	19	000019	19	000019
20	000020	20	000020	20	000020	20	000020	20	000020
21	000021	21	000021	21	000021	21	000021	21	000021
22	000022	22	000022	22	000022	22	000022	22	000022
23	000023	23	000023	23	000023	23	000023	23	000023
24	000024	24	000024	24	000024	24	000024	24	000024
25	000025	25	000025	25	000025	25	000025	25	000025
26	000026	26	000026	26	000026	26	000026	26	000026
27	000027	27	000027	27	000027	27	000027	27	000027
28	000028	28	000028	28	000028	28	000028	28	000028
29	000029	29	000029	29	000029	29	000029	29	000029
30	000030	30	000030	30	000030	30	000030	30	000030
31	000031	31	000031	31	000031	31	000031	31	000031
32	000032	32	000032	32	000032	32	000032	32	000032
33	000033	33	000033	33	000033	33	000033	33	000033
34	000034	34	000034	34	000034	34	000034	34	000034
35	000035	35	000035	35	000035	35	000035	35	000035
36	000036	36	000036	36	000036	36	000036	36	000036
37	000037	37	000037						



The diagram illustrates a transmitter system with a feedback loop for distortion compensation. The system components and their interconnections are as follows:

- Transmit-Signal Generator (21):** Generates the initial transmit signal.
- S/P Converter (31):** Converts the signal from serial to parallel.
- Multiplexer (24):** Combines the signal from the S/P converter with a feedback signal (29) to produce the **MPL** signal.
- D/A Converter (32):** Converts the MPL signal into an analog signal.
- Modulator (26):** Modulates the analog signal.
- Amplifier (27):** Amplifies the modulated signal.
- Antenna (28):** Transmits the amplified signal.
- Feedback Path (29):** Receives the transmitted signal and feeds it back to the multiplexer (24).
- Distortion Compensation Coefficient Table RAM (22):** Stores pre-stored distortion compensation coefficients.
- Distortion Compensation Coefficient Updating Unit (25):** Updates the coefficients in the RAM based on the output of the rotation calculation unit (43). It includes:
 - Amplitude-to-Power Converter (23a):** Converts the output of the rotation calculation unit (43) into a power signal $P(t)$.
 - Summing Junctions (23c', 23c''):** Calculate the differences ΔP and $\Delta P'$ between the current power and the stored coefficients.
 - Delays (23b', 23d):** Store and delay the calculated differences.
- Distortion Compensation Coefficient Table RAM (22):** Receives the updated coefficients from the updating unit (25) and provides them to the multiplexer (24) and the rotation calculation unit (43).
- Rotation Calculation Unit (43):** Calculates the rotation angle μ based on the input signal and the coefficients from the RAM.
- Summing Junction (42):** Combines the output of the rotation calculation unit (43) with the output of the delay unit (41) to produce the final output signal.
- Delay Unit (41):** Delays the output signal for feedback.
- A/D Converter (33):** Converts the output signal into a digital signal.
- Demodulator (30):** Demodulates the digital signal to produce the feedback signal (29).

FIG. 18

$P(t)$	ΔP	$\Delta P'$	$h(P(t), \Delta P, \Delta P')$
P_1	ΔP_1	ΔP_1	$h(P_1, \Delta P_1, \Delta P_1)$
		ΔP_2	$h(P_1, \Delta P_1, \Delta P_2)$
		\vdots	\vdots
		ΔP_n	$h(P_1, \Delta P_1, \Delta P_n)$
	ΔP_2	ΔP_1	$h(P_1, \Delta P_2, \Delta P_1)$
		ΔP_2	$h(P_1, \Delta P_2, \Delta P_2)$
		\vdots	\vdots
		ΔP_n	$h(P_1, \Delta P_2, \Delta P_n)$
	\vdots	\vdots	\vdots
	ΔP_n	ΔP_1	$h(P_1, \Delta P_n, \Delta P_1)$
		ΔP_2	$h(P_1, \Delta P_n, \Delta P_2)$
		\vdots	\vdots
		ΔP_n	$h(P_1, \Delta P_n, \Delta P_n)$
P_2	ΔP_1	ΔP_1	$h(P_2, \Delta P_1, \Delta P_1)$
		ΔP_2	$h(P_2, \Delta P_1, \Delta P_2)$
		\vdots	\vdots
		ΔP_n	$h(P_2, \Delta P_1, \Delta P_n)$
\vdots	ΔP_2		
\vdots	\vdots	\vdots	\vdots
P_m			

FIG. 19

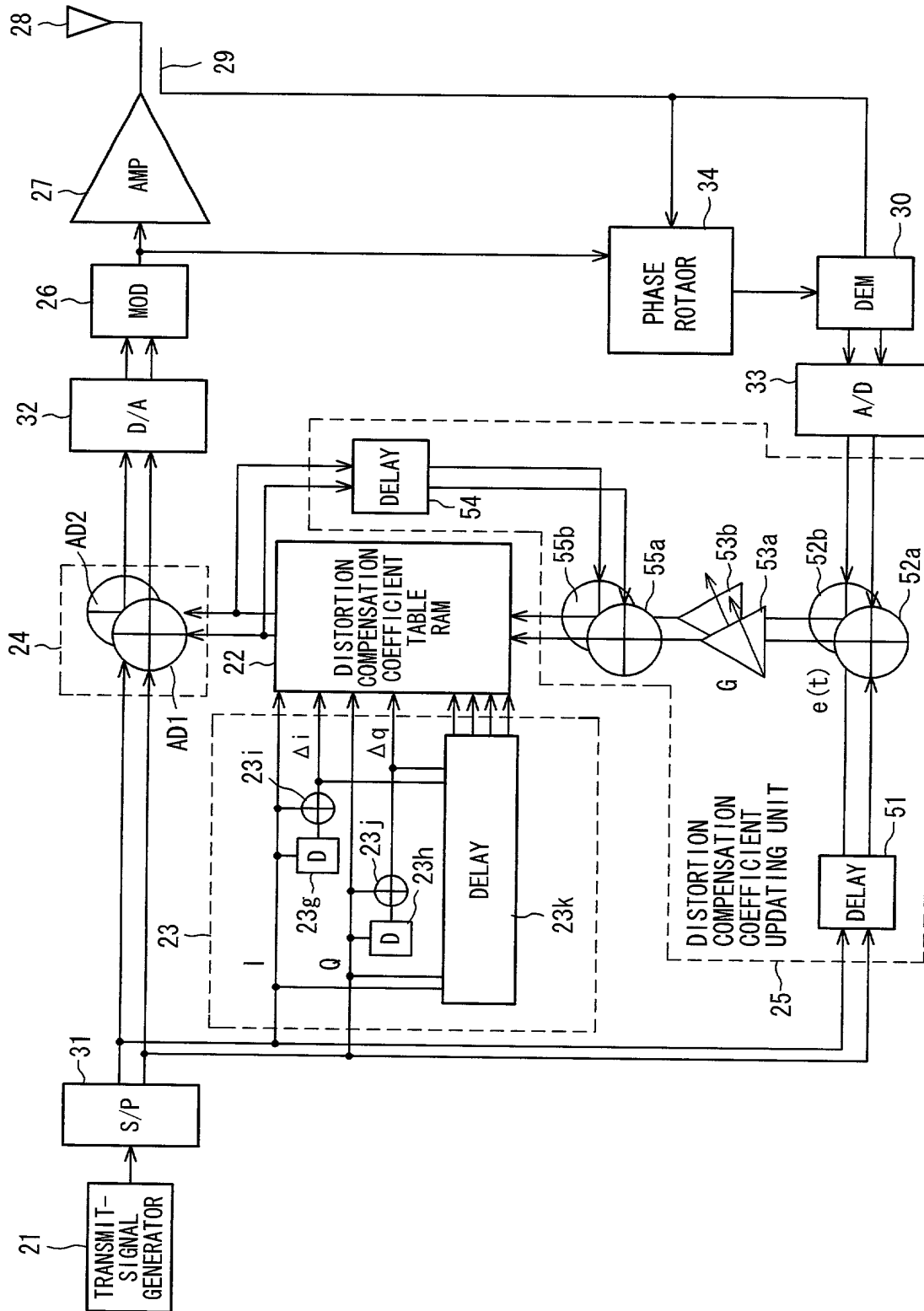


FIG. 20

(a)

$I(t)$	Δi	$hi(I(t), \Delta i)$
I_1	Δi_1	$hi(I_1, \Delta i_1)$
	Δi_2	$hi(I_1, \Delta i_2)$
	Δi_3	$hi(I_1, \Delta i_3)$
	\vdots	\vdots
	Δi_n	$hi(I_1, \Delta i_n)$
I_2	Δi_1	$hi(I_2, \Delta i_1)$
	Δi_2	$hi(I_2, \Delta i_2)$
	Δi_3	$hi(I_2, \Delta i_3)$
	\vdots	\vdots
	Δi_n	$hi(I_2, \Delta i_n)$
I_3	\vdots	\vdots
I_m	Δi_1	$hi(I_m, \Delta i_1)$
	Δi_2	$hi(I_m, \Delta i_2)$
	Δi_3	$hi(I_m, \Delta i_3)$
	\vdots	\vdots
	Δi_n	$hi(I_m, \Delta i_n)$

(b)

$Q(t)$	Δq	$hq(Q(t), \Delta q)$
Q_1	Δq_1	$hq(Q_1, \Delta q_1)$
	Δq_2	$hq(Q_1, \Delta q_2)$
	Δq_3	$hq(Q_1, \Delta q_3)$
	\vdots	\vdots
	Δq_n	$hq(Q_1, \Delta q_n)$
Q_2	Δq_1	$hq(Q_2, \Delta q_1)$
	Δq_2	$hq(Q_2, \Delta q_2)$
	Δq_3	$hq(Q_2, \Delta q_3)$
	\vdots	\vdots
	Δq_n	$hq(Q_2, \Delta q_n)$
Q_3	\vdots	\vdots
Q_n	Δq_1	$hq(Q_m, \Delta q_1)$
	Δq_2	$hq(Q_m, \Delta q_2)$
	Δq_3	$hq(Q_m, \Delta q_3)$
	\vdots	\vdots
	Δq_m	$hq(Q_m, \Delta q_n)$

FIG. 21

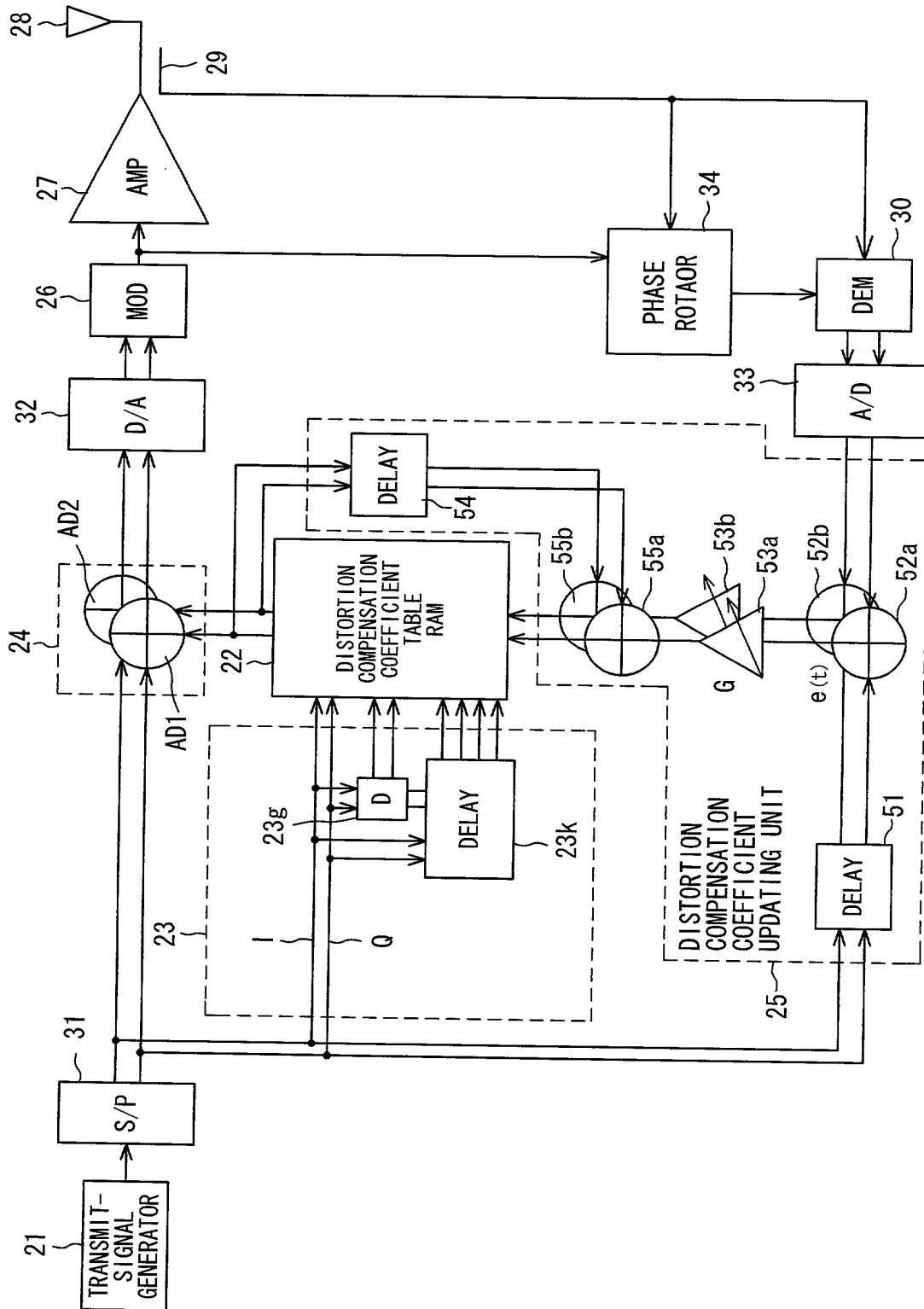


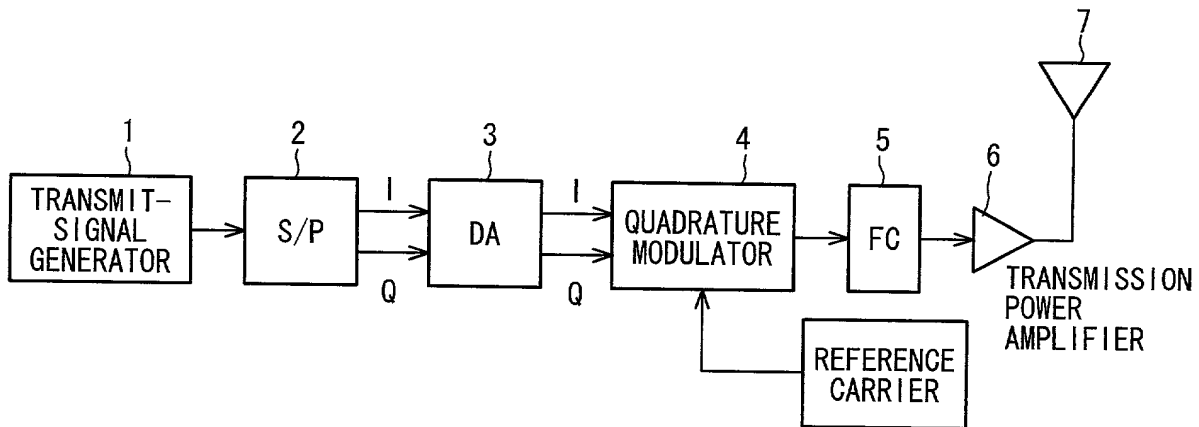
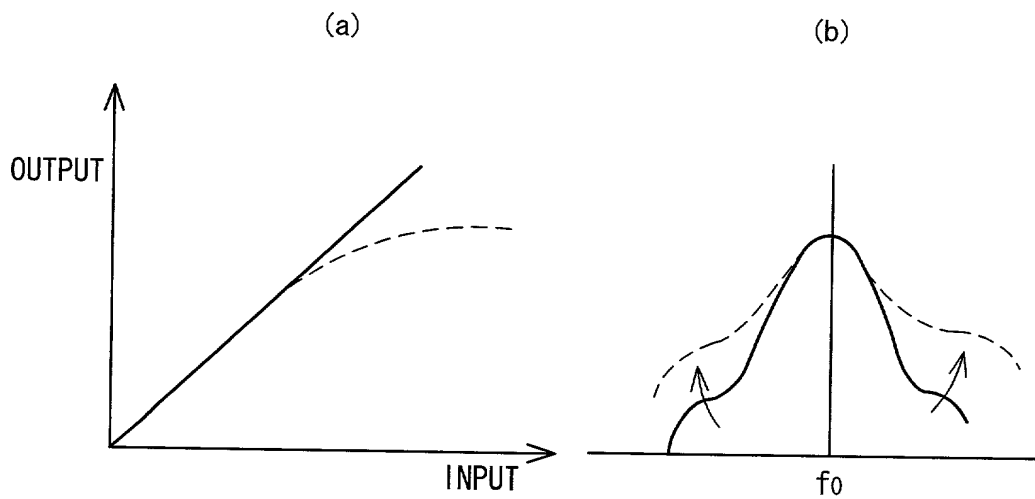
FIG. 22**FIG. 23**

FIG. 24

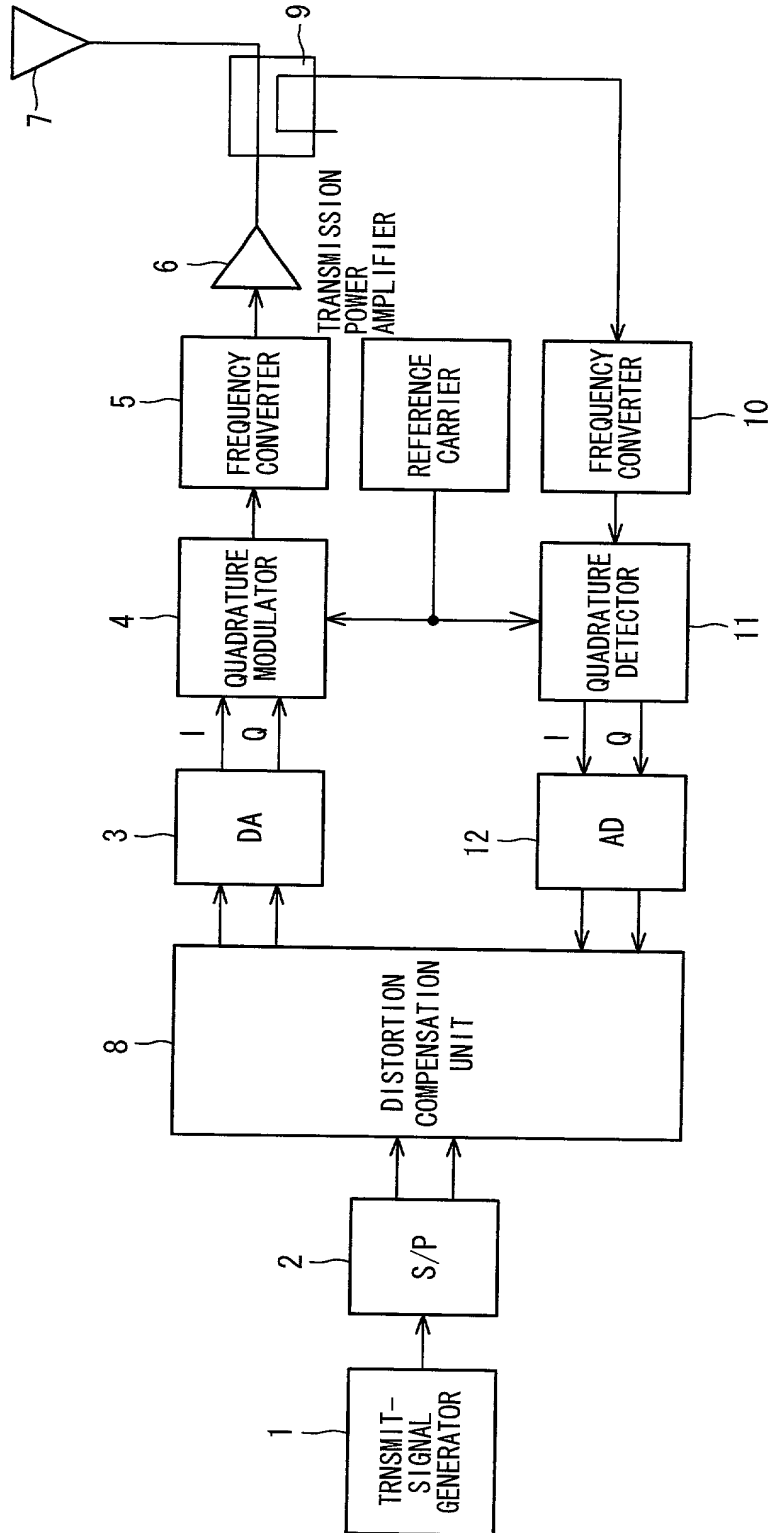


FIG. 25

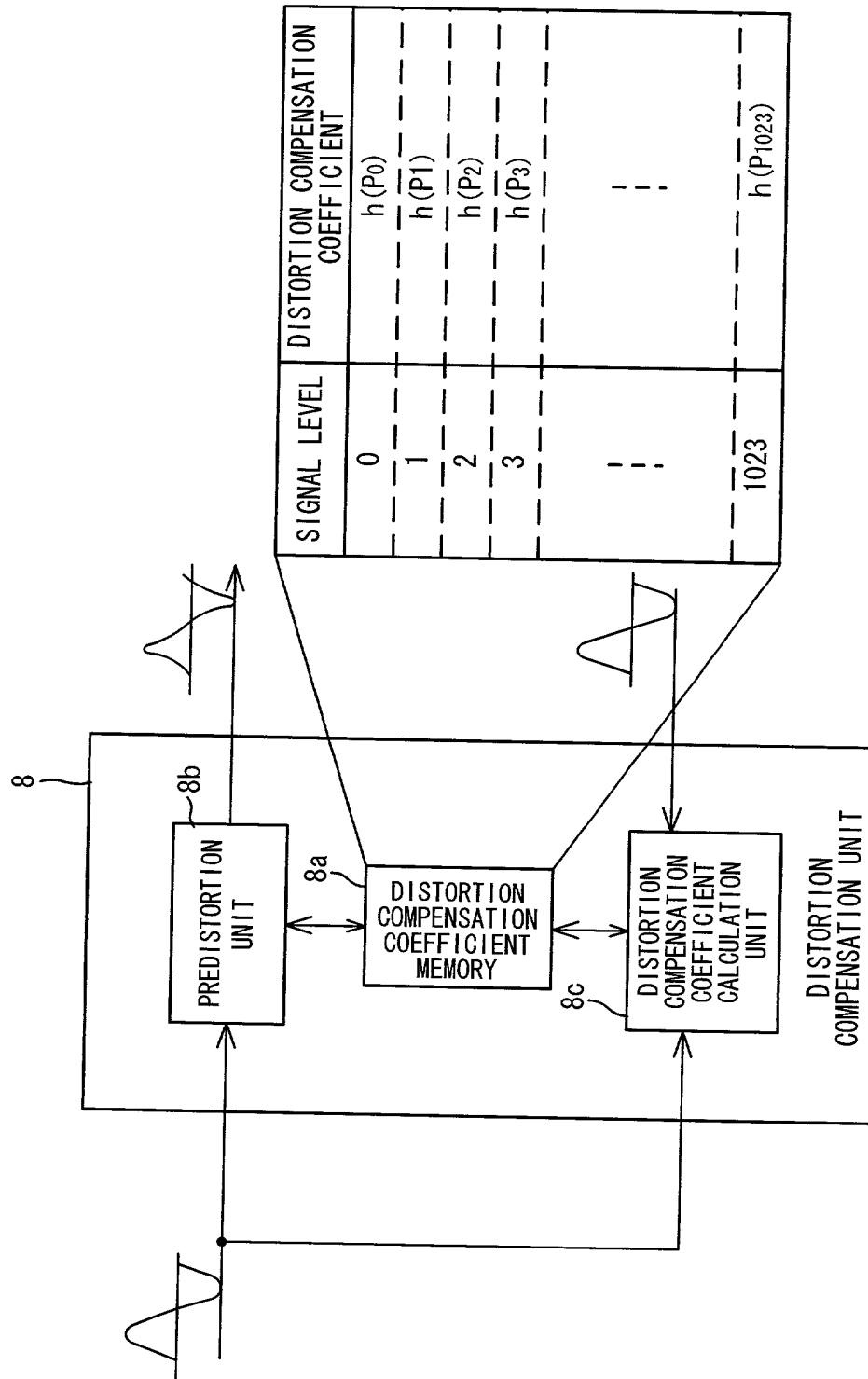


FIG. 26

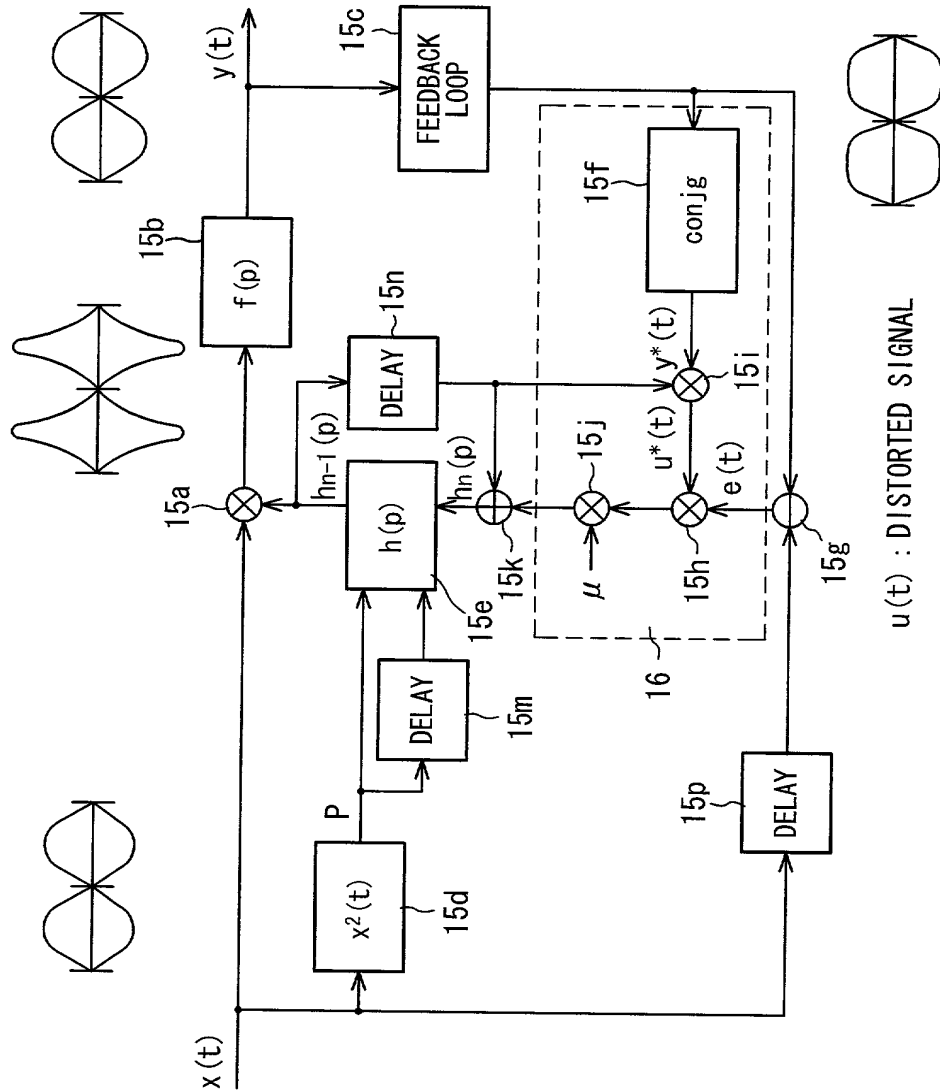


FIG. 27

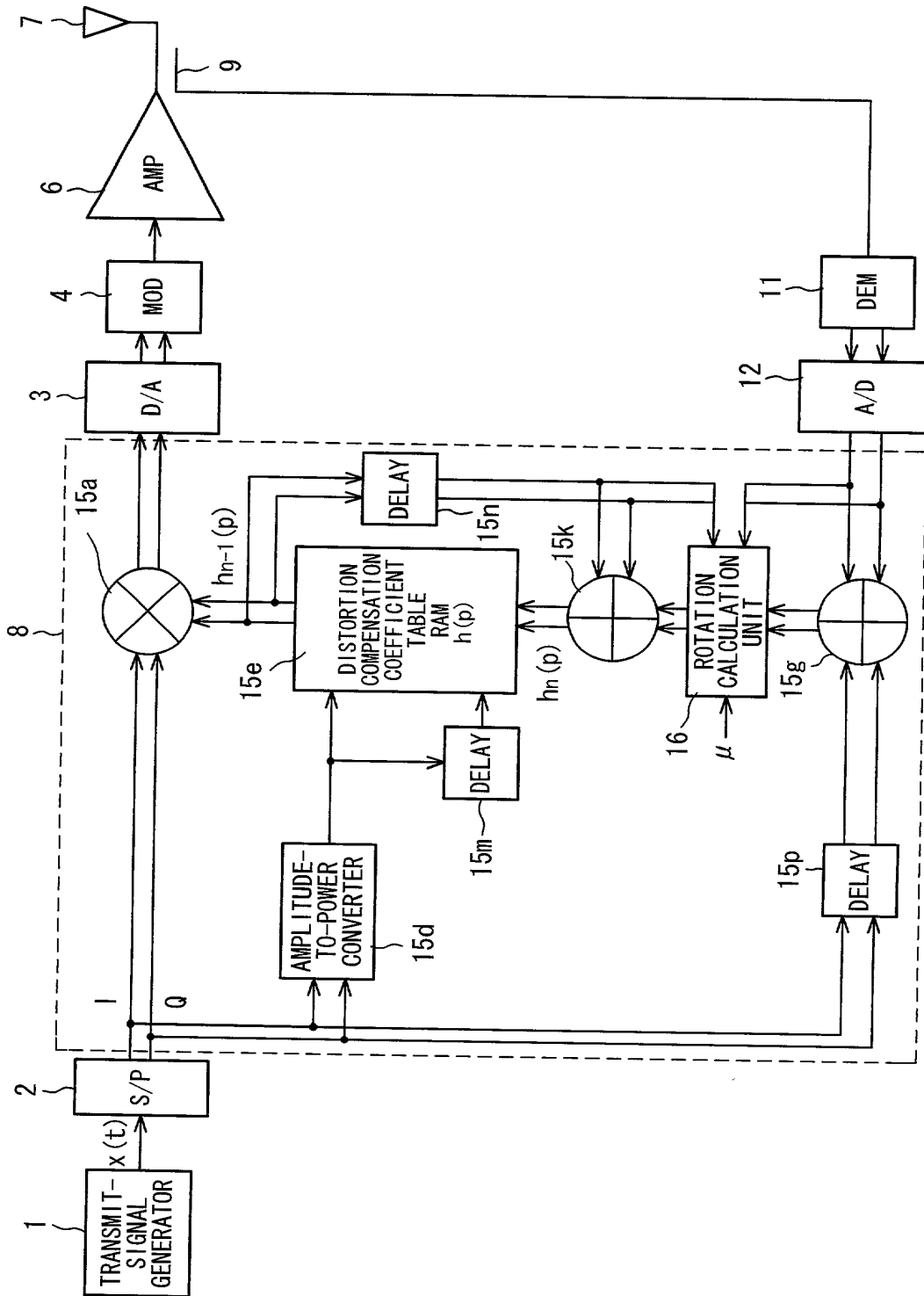


FIG. 28